A Highly-Integrated 3–8 GHz Ultra-Wideband RF Transmitter With Digital-Assisted Carrier Leakage Calibration and Automatic Transmit Power Control

Horng-Yuan Shih, *Member, IEEE*, and Chih-Wei Wang

***Abstract*—This paper presents a highly-integrated 3–8 GHz ultra-wideband (UWB) RF transmitter implemented in a 1.2 V 0.13-μm CMOS technology. The transmitter integrates an analog baseband (PGAs and filter), an IQ modulator, a variable gain amplifier (VGA), a differential-to-single-ended amplifier, a power amplifier, as well as a transmitted signal strength indicator (TSSI). The RF VGA and the TSSI cooperate to perform an automatic transmit power control. The IQ modulator and an off-chip digital circuit implemented by a FPGA perform a carrier leakage calibration. Measured maximum output power and OP1 dB are −5 and +1.5 dBm, respectively. Measured worst carrier leakage suppression is 21 dB (before calibration) at 6.6 GHz. Measured worst sideband suppression is 29.1 dB at 7.6 GHz. The high linearity and accurate IQ modulation lead to an error vector magnitude (EVM) of −28 dB under the data rate of 480 Mb/s in WiMedia Mode 1. The entire transmitter consumes 66 mW under supply voltage of 1.2 V.**

***Index Terms*—Carrier leakage calibration, RF transmitter, transmit power control, ultra-wideband (UWB).**

I. Introduction

FEDERAL COMMUNICATIONS COMMISSION (FCC) approved the ultra-wideband (UWB) standard for commercialization in February 2002. To avoid interfering the existing narrowband communication systems, the transmit power spectral density level is limited to −41.3 dBm/MHz [1]. Low transmit power leads UWB to be suitable for wireless personal area network (WPAN) applications. One of the UWB systems is the multi-band (MB)-OFDM UWB which, proposed by WiMedia/MBOA alliance, divides the frequency spectrum of 3.1–10.6 GHz into five band groups [2]. Band group 1 (3.2–4.7 GHz) has the first priority, while the others are reserved for further usage. But the frequency spectrum of Band group 1 overlaps with that of WiMax, which was recently proposed for wireless metropolitan area network (WMAN) applications. As to Band Group 2, allocated in the frequency band of 4.8–6.3 GHz, it also interferes with WLAN 802.11a. The strong interference in Band Group 1 and Band Group 2 seriously degrades the link quality of UWB networks. On the contrary, no other commercial radio system has been assigned to the spectrum of Band Group 3 (6.3–8 GHz). Using this frequency band potentially has better link quality to realize a higher data rate.

UWB system may be integrated with other communication systems in a same platform for providing a short range and high data rate service. In order to avoid to interfere with other communication systems, the transmit power of a UWB transmitter should be restricted within a level which will not degrade signal-to-noise ratio (SNR) of other communication systems and can still have enough link quality for communicating with other UWB devices. Therefore, an automatic power control loop is essential in a UWB transmitter for controlling output power precisely. Otherwise, DC-offset of IQ modulator in a transmitter leads to a serious problem of carrier leakage which not only saturates UWB receivers but also interfere other communication systems. Therefore, a carrier leakage calibration is needed in a UWB transmitter.

In this paper, a highly-integrated 3–8 GHz wideband RF transmitter with a digital-assisted carrier leakage calibration and an automatic transmit power control is implemented in a 1.2 V 0.13-μm CMOS process. This paper is organized as follows. Section II describes the architecture and specifications of the wideband RF transmitter. Section III describes design details of the circuits. In Section IV, measurement results are presented. Section V concludes this work.

II. Architecture and Specifications

The architecture of the proposed transmitter is as shown in Fig. 1, which carries out the direct-conversion architecture, including an analog baseband (PGAs and filter) and a RF up-converter. The analog baseband featured wide bandwidth of 250 MHz is consisted of a 6th-order Chebyshev low-pass filter and baseband PGAs. The RF up-converter designed to cover from 3 to 8 GHz is composed by an IQ modulator, a RF VGA, a differential-to-single-ended (D-to-S) amplifier and a power amplifier (PA). An automatic transmit power control (ATPC) is consisted of a TSSI, the RF VGA, a off-chip analog-to-digital converter (ADC), a off-chip digital-to-analog converter (DAC), and a digital counter. Analog portions of the ATPC are integrated in this chip, and digital portions of the ATPC are implemented by a

Manuscript received February 11, 2011; revised April 28, 2011; accepted May 17, 2011. Date of publication June 27, 2011; date of current version June 14, 2012. This work was supported by the National Science Council, Taiwan, R.O.C., under Grant NSC-99-2218-E-032-007.

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Digital Object Identifier 10.1109/TVLSI.2011.2157842

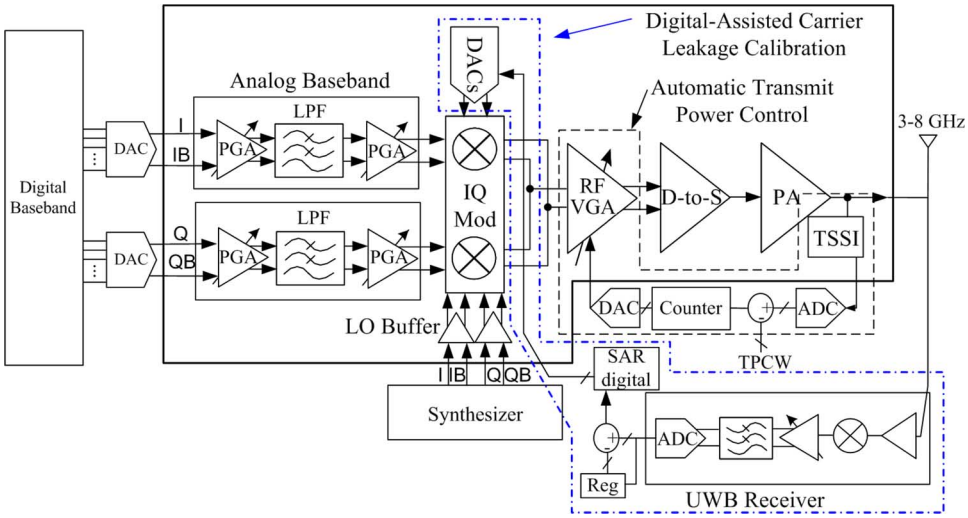

Fig. 1. Block diagram of the wideband RF transmitter.

TABLE I
LINK BUDGET OF TRANSMITTER

DAC output swing	125 mV_p — 375m V_p (-18 dBV — -8.5 dBV)
Gain of analog Baseband	-9 dB — -19 dB
Modulator input swing	-27 dBV
Gain of RF stages	9.5 dB
Output power of transmitter	-7.5 dBm

TABLE II
SPECIFICATIONS

Analog Baseband	Bandwidth: 250 MHz
	Gain: -9 dB — -19 dB
	Gain resolution: 1 dB
	THD: -40 dBc
	Attenuation: 285 MHz: 12 dB 330 MHz: 20 dB
RF circuits	Gain: 9.5 dB
Overall Tx	Pout, max: -7.5 dBm
	OP1dB: +1.5 dBm
	Carrier Suppression > 31 dBc
	Sideband Suppression > 30 dBc
	Power control range: 14 dB

field-programmable gate array (FPGA). A digital-assisted carrier leakage calibration (DACLC) is composed of DACs in the IQ modulator, a digital control logic implemented in the FPGA and an additional receiver chain.

At the baseband signal input, the low-pass filter eliminates the output harmonics from a baseband digital-to-analog converter (BBDAC). The baseband PGAs provide tunable attenuation from 9 to 19 dB to adjust the signal amplitude to a properly pre-determined level for the IQ modulator. The IQ modulator is designed to modulate baseband signals to RF frequency. A DC-offset cancellation circuit is integrated for improving the performance of carrier leakage suppression. The RF VGA provides linear-in-dB gain tuning of 14 dB. The D-to-S amplifier is designed before the single-ended power amplifier for combining differential signals with an acceptable gain and phase error from 3 to 8 GHz. Finally, the power amplifier is designed to boost the RF signals and linearly drive the 50 Ω antenna load.

Interfacing with the digital baseband, the BBDAC generates modulated signals with a sufficient spurious-free dynamic range (SFDR) to meet the system requirement. Then the RF transmitter performs I+jQ to combine in-phase and quadrature-phase signals from the BBDAC and up-converts the modulated signals to the RF frequency. But the RF transmitter introduces unwanted effect on the output signals such as carrier leakage, sideband leakage and distortions simultaneously. The SNR is the most important parameter to receiver design. However, the key parameter of transmitter design is the signal-to-spur ratio (SSR). The carrier leakage, sideband leakage and distortions all lead to SSR degradation.

According to the FCC regulation, the output power spectrum density of UWB is limited to -41.3 dBm/MHz. The maximum in-band signal power is calculated as

$$-41.3 \text{ dBm/MHz} + 10 \cdot \text{LOG}_{10}(3 \times 528 \text{ MHz}) = -10 \text{ dBm}. \quad (1)$$

The transmitter output power should be up to -7.5 dBm assuming the signal attenuation is 2.5 dB due to the transmit/receive (T/R) switch at the transmitter output. Listed in Table I is the transmitter link budget, which is designed for best SSR performance. The input voltage swing to this transmitter, or the output voltage swing from a BBDAC, is assumed in the range from 125 to 375 mVp for a flexible BBDAC interface. Large input voltage swing of the IQ modulator leads to better carrier/sideband leakage suppression performance but also leads to harmonic distortions. For the optimal SSR performance of the

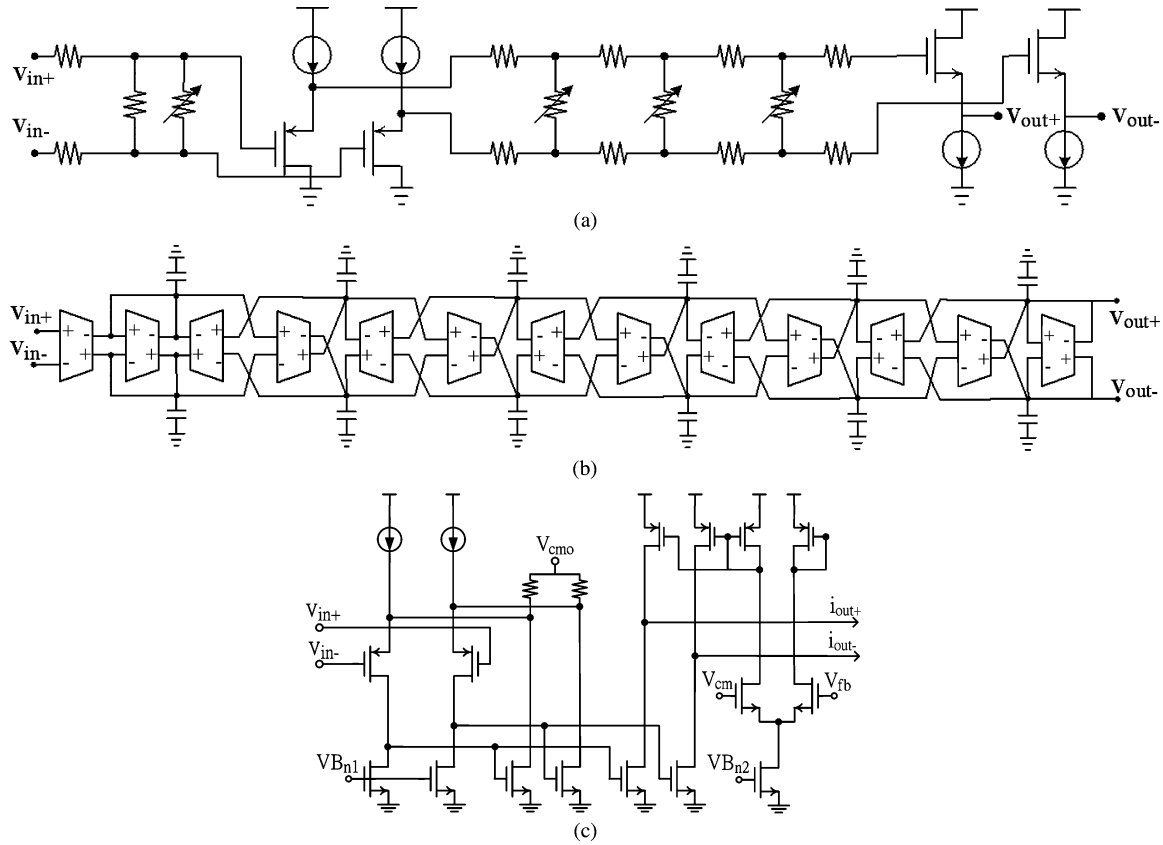

Fig. 2. Schematic of the ABB (a) PGA (b) low-pass filter. (c) Gm cell.

IQ modulator, the input voltage swing at the modulator input is fixed at 44.6 mV (−27 dBV). It requires gain tuning from −9 to −19 dB in the analog baseband. Thus, it is specified a gain tuning range of 10 dB with the resolution of 1 dB. The RF circuits following the analog baseband provide 9.5 dB gain for the maximum output power of −7.5 dBm.

Peak-average ratio (PAR) of an OFDM signal determines on how many sub-carriers used in a channel, which leads to PAR of 9 dB in MB-OFDM UWB system. Transmitter linearity is constrained by the PAR of 9 dB, which leads to an instantaneous power increase of 9 dB. Therefore, the RF transmitter should have the ability to linearly transmit signals as large as +1.5 dBm (−7.5 dBm + 9 dB). Consequently the required OP1 dB should be over +1.5 dBm. The carrier leakage emission is also strictly regulated within −41.3 dBm. Thus, the required carrier leakage suppression is derived as

$$-10\ \text{dBm} - (-41.3\ \text{dBm}) = 31.3\ \text{dBc}. \tag{2}$$

The leakage is lumped to the effect caused by DC offset. Since the voltage swing at the IQ modulator input is 44.6 mV (−27 dBV), the input-referred DC-offset of the IQ modulator should be less than 1.21 mV (−58.3 dBV). This small level requires a DC-offset calibration circuit. According to the transmit spectrum mask specified by MB-OFDM UWB, the filter in the analog baseband should provide at least out-of-band attenuation of 12 and 20 dB at the frequencies of 285 and 330 MHz, respectively. The design specification of the MB-OFDM UWB RF transmitter is listed in Table II.

III. Circuit Design

A. Analog Baseband (ABB)

The ABB is consisted of a programmable gain amplifier (PGA), a 6th-order low-pass filter (LPF) and a voltage amplifier for buffering proposes. Fig. 2(a) shows the schematic of the PGA. The switched-resistor PGA features low power consumption and provides gain tuning range of 10 dB to adjust the output amplitude of the BBDAC for enlarging SSR performance of an IQ modulator following the ABB. Fig. 2(b) shows the schematic of the 6th-order LPF. The LPF based on Gm-C architecture is biased under a small current for low power consumption. The schematic of the Gm cell is as shown in Fig. 2(c). The super source follower structure as in [3] is applied to improve the linearity of the Gm cells under a low bias current. The super source follower structure also features high common-mode rejection ratio (CMRR) that immunizes to supply and subtract noise. Regulated by the gain-bandwidth product limit, the Gm-C filter is therefore designed with no gain to extend its bandwidth to 250 MHz. Finally, a voltage amplifier is composed of a super source follower and a normal source follower for buffering output signals of the LPF. Owing to every Gm cell is designed only consumed 250 μA, the total current consumption of the LPF including the buffer is 3.75 mW. Two parallel LPFs are needed for in-phase and quadrature-phase paths which result in a current consumption of 7.5 mA. Otherwise, the PGA consumes 400 μA for each phase. Therefore, the total power consumption of the ABB is about 10 mW under a supply voltage of 1.2 V.

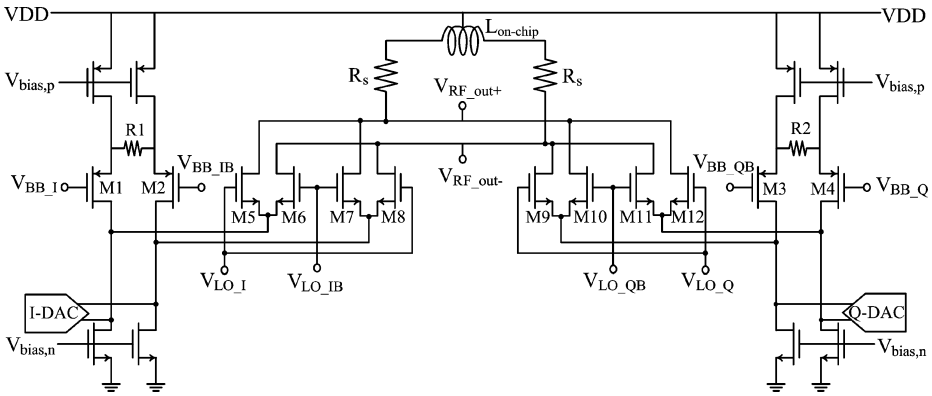

Fig. 3. Schematic of the IQ modulator.

B. IQ Modulator

Fig. 3 shows the schematic of the IQ modulator. The IQ modulator modulates the BB IQ signals up to a differential RF signal by multiplying a RF IQ local oscillation (LO) signal. For low voltage operation, a folded configuration is adopted to ensure sufficient voltage headroom for trans-conductor and switching cells. In order to further increase linearity of the modulator, resistive degeneration is adopted in the input trans-conductor cells. The modulator load is shunt inductive peaking with on-chip series resistor to enlarge bandwidth for covering 3–8 GHz. The on-chip inductor is center-tapped type with inductance of 3 nH. The modulator modulates BB signals into a RF signal and provides no conversion gain. The power consumption of the modulator is 4 mW.

Mismatch of circuits leads to unwanted carrier and sideband leakage. Carrier leakage is mainly contributed by DC-offset between differential circuits. However, sideband leakage is coming from amplitude and phase mismatch between BB IQ signals or RF IQ LO signals. Carrier leakage can be reduced by using a DC-offset calibration (DCOC) circuit in the RF transmitter. Otherwise, sideband leakage can be decreased by compensating the amplitude and phase mismatch of BB IQ signals in digital baseband of the transmitter.

DC-offset in the IQ modulator leads to unwanted carrier leakage, which saturates receivers. The main DC-offset contributors are trans-conductor cells and bias current sources of the modulator. The input-referred DC-offset due to trans-conductor cells had been formulated as follows [4]

$$V_{\text{in,offset}} = \Delta V_{\text{th}} + \frac{V_{\text{ov}}}{2} \times \frac{\Delta\left(\frac{W}{L}\right)}{\frac{W}{L}} + \frac{\text{IR}_s}{2} \times \frac{\Delta I}{I} \qquad (3)$$

where W/L, V_{th}, I and V_{ov} are the device size, threshold voltage, bias current and over-drive voltage of the trans-conductor cells (M1–M4), respectively. R_s denotes the degenerative resistance, R1 and R2. In the trans-conductor cells, the effect of transistor size mismatch is amplified by over-drive voltage (V_{ov}). Threshold voltage mismatch directly contributes DC-offset. Large transistors can be used to decrease V_{ov} Otherwise, well-matched layout leads to reduce mismatch of threshold voltage. In the last term of (3), resistive degeneration in the trans-conductor cells amplifies the effect of current mismatch. Thus, resistance of degeneration is designed to tradeoff between DC-offset and linearity. Mismatch among biasing current sources is alleviated by using large transistors, each with a fixed gate length of 2 μm and a total gate width larger than 500 μm and well-matched layout in this design. The mismatches of the switching cells also introduce carrier leakage. A symmetrical layout for the switching cells is important as well.

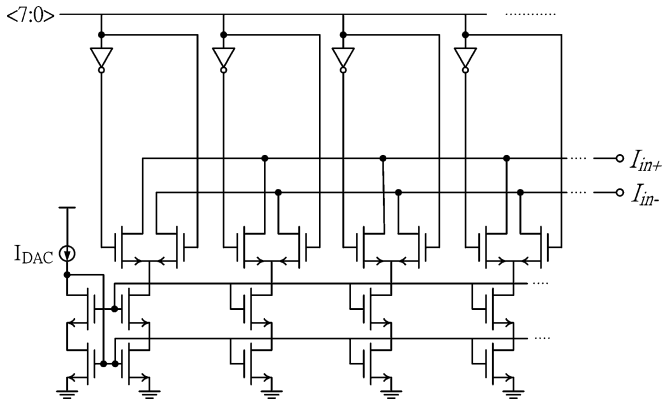

Fig. 4. Schematic of the current-steering based DAC.

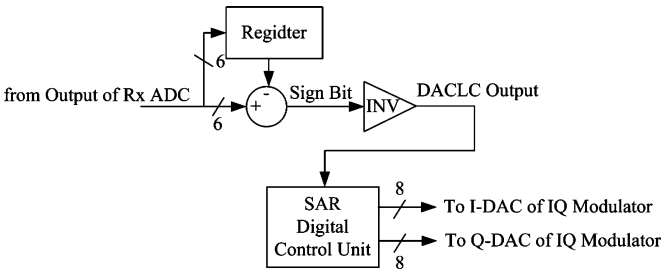

Fig. 5. Schematic of the DACLC.

C. Digital-Assisted Carrier Leakage Calibration (DACLC)

For additional carrier leakage reduction, the modulator also incorporates a calibration mechanism. The DACLC function is realized by cooperating of two DACs (one DACs for I channel, and one DACs for Q channel) in the modulator, a digital control unit implemented in a FPGA and an additional receiver chain. Carrier leakage owing to I channel and Q channel are calibrated separately. The Carrier leakage calibration range and resolution are dependent on number of bits and LSB current of the DACs. In this design, 8-bit DACs with a LSB current of 0.5 μA are adopted. The 8-bit DACs based on a current-steering

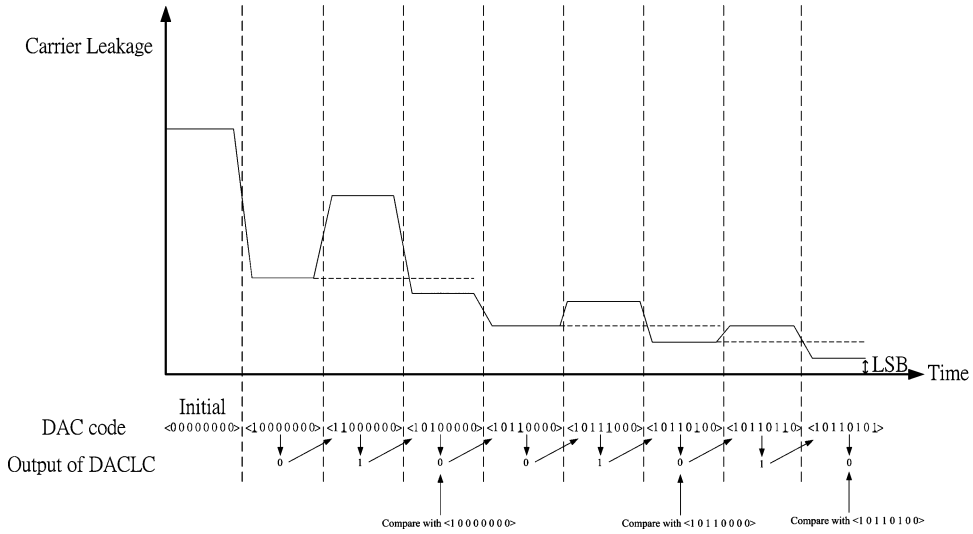

Fig. 6. Example of the SAR carrier leakage calibration.

structure draw currents out the modulator bias branches to balance the DC-offset for cancelling the carrier leakage as shown in Fig. 3. The impedance of current drawn node decided by g_m of switching cells in the modulator is 250 Ω. Therefore, a 8-bit DAC with LSB of 0.5 μA leads to DC-offset calibration range of 63.875 mV and resolution of 0.125 mV. The schematic of the current-steering-based DAC is shown in Fig. 4.

As performing the DACLC, BB signals are turned off. As shown in Fig. 5, an additional receiver chain is used to sense the strength of the output carrier leakage and converts it into a digital code. In order to compare the strength of carrier leakage of different DAC settings, a substrater is used to subtract the outputs of the ADC between different DAC settings. As sign bit of the output of the substrater is "0" that means the output of the substrater is a positive value owing to the strength of carrier leakage increases. On the contrary, as sign bit of the output of the substrater is "1" that means the output of the substrater is a negative value owing to the strength of carrier leakage decreases. Finally, an inverter is adopted to invert the sign bit of the output of the substrater. Therefore, as the output of the inverter is "0" that means the strength of carrier leakage decreases. On the contrary, as the output of the inverter is "1" that means the strength of carrier leakage increases.

Initially, the DAC is set as $\langle 0,0,0,0,0,0,0,0\rangle$. A digital control logic implemented in a FPGA performs successive approximation (SAR) search to set the DAC according to the output of the DACLC. Fig. 6 shows an example of the carrier leakage calibration procedure. Then, the DAC is set as $\langle 1,0,0,0,0,0,0,0\rangle$, which leads to draw one more LSB current out one of balanced branches of the modulator. The output of the DACLC is "0". This means the strength of carrier leakage decreases. For eliminating the carrier leakage, by SAR method, the DAC is re-set as $\langle 1,1,0,0,0,0,0,0\rangle$ by the digital control logic unit. This means that the DAC steals more current from the "$-$' branch of modulator (less current from the '$+$" branch of modulator). After that, the output of the DACLC becomes "1", which means output DC at the "$-$" branch of modulator is lower than that of the "$+$" branch. Then, the DAC is re-set as $\langle 1,0,1,0,0,0,0,0\rangle$ by the digital control logic unit to steal more current from the "$+$" branch of modulator, and so on. After the eight bits of DAC are set, the carrier leakage of the modulator is calibrated to the minimum carrier leakage limited by the LSB current of DAC, which consumes time of eight clock cycles. Every one bit SAR search needs two clock periods, one clock period for DACLC and the other one clock period for digital control unit to control the DAC. As the reference clock of 20 MHz is used, the time consumed by calibrating carrier leakage owing to one channel of the modulator only needs 0.8 μs. Therefore, only 1.6 μs is need for both I-channel and Q-channel of the modulator.

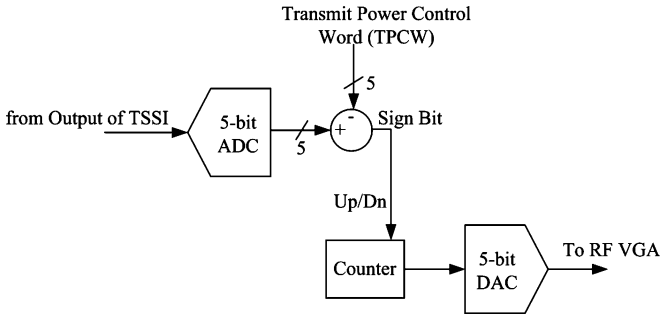

Fig. 7. Schematic of the ATPC.

D. Automatic Transmit Power Control (ATPC)

As shown in Fig. 7, an ATPC is consisted by a TSSI, a RF variable gain amplifier (VGA), an off-chip 5-bit ADC, an off-chip 5-bit DAC, and a Up/Dn counter. The TSSI senses the output transmitted power and converts it into a voltage. The 5-bit ADC converts the output voltage of the TSSI into a digital code which substrates by a transmit power control word (TPCW). Then, the result is used to control the counter. Finally, the output of the counter is converted into a voltage by the 5-bit DAC for controlling the RF VGA. Therefore, the resolution of the ATPC is depended on the resolution of the ADC and DAC.

Fig. 8 depicts the schematic of the approximated linear-in-dB variable gain amplifier (VGA). It consists of a cascoded differential amplifier (M6–M7) with inductively peaked resistive loads to broaden the output bandwidth. Continuous analog gain

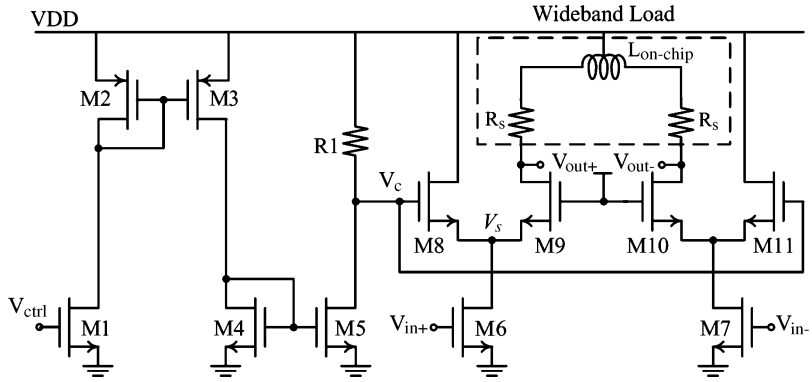

Fig. 8. Schematic of variable gain amplifier.

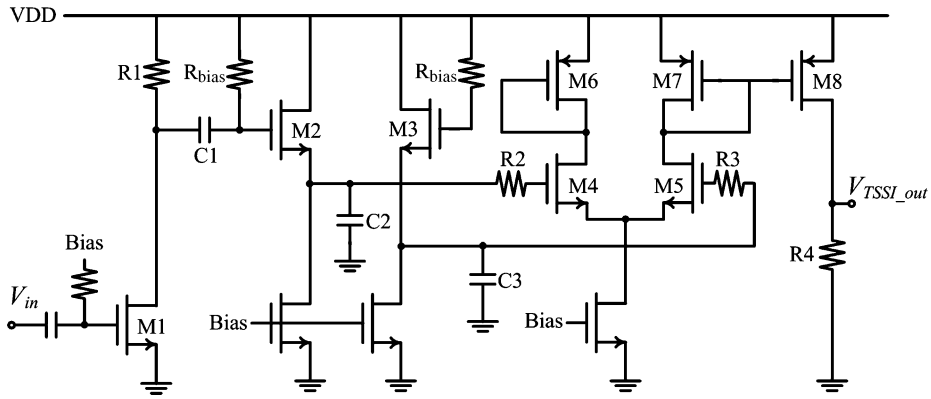

Fig. 9. Schematic of TSSI.

control is achieved by current steering cells (M8–M11), controlled by a voltage transformation circuit (M1–M5 and R1) that regulates the input control voltage (Vctrl). In order to realize linear-in-dB power control, the voltage transformation circuit translates the input control voltage exponentially to Vc as M1 operated in subthreshold region [5]

$$VDD - V_c = e^{K \cdot V_{\rm ctrl}} \tag{4}$$

where K is $R_1 \cdot \mu_n \cdot C_{\rm ox} \cdot (W/L)_1$.

Current gain of the current steering cells (M8–M11) is tuned by Vc as

$$G_i = \frac{W_8}{W_9 \cdot (VDD - V_s - V_{\rm th})} \cdot (VDD - V_c). \tag{5}$$

Therefore, according to (4) and (5), voltage gain of the RF VGA is expressed as

$$G_v = \frac{Z_L \cdot W_8}{W_9 \cdot (VDD - V_s - V_{\rm th})} \cdot e^{K \cdot V_{\rm ctrl}}. \tag{6}$$

Owing to the current steering adopted in the cascade stage, constant bias current in the input stage (M6–M7) avoids linearity degradation during gain variation. The on-chip inductor used in the RF VGA is center-tapped type with inductance of 3 nH. The power consumption of the RF VGA is 8 mW.

In Fig. 9, an on-chip transmitted signal strength indicator (TSSI) is implemented to measure the transmitter output power. The TSSI consists of three stages. The first stage is a voltage amplifier (M1 and R1) that increases the detecting sensitivity. The second stage is a peak detector (M2 and C2) configured as a source follower with a capacitive load. The equivalent 1/gm resistor provided by M2 is connected in series to the capacitive load (C2) to form a RC rectifier for detecting the RMS voltage of the incoming RF signals. M3 and C3 are used to provide a reference voltage. The third stage is a comparator (M4–M7 and R2–R3) that compares the root-mean-square voltage of the incoming RF signals with the reference voltage. Finally, M8 and R4 are used to transform the output current of the comparator into an output voltage.

The setting time of the ATPC is mainly depended on sampling clock and resolution of the ADC and the DAC, sensing gain (SG) of the TSSI and tuning gain (TG) of the RF VGA. In this design, the SG and TG are designed as 15 and 20 dB/V. Owing to the sampling clock of the ADC and DAC are 20 MHz, it needs 0.05 μs for a tuning step. Considering the worst condition, there is a maximum gain control of 14 dB. The maximum setting time can be calculated as

$$T_{\rm setting} = \frac{14}{15} \cdot 20 \cdot 2^5 \cdot 0.05\mu \approx 32\ \mu{\rm s}. \tag{7}$$

E. Differential to Single-Ended (D-to-S) Amplifier and Power Amplifiers

A broadband gain buffer is used to perform the differential to single-ended conversion, as shown in Fig. 10. The inductor serves as a shunt peaking component for the common-source stage (M1) and also as a series peaking element for the source

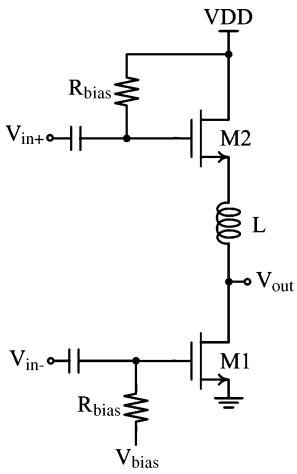

Fig. 10. Schematic of the D-to-S voltage amplifier.

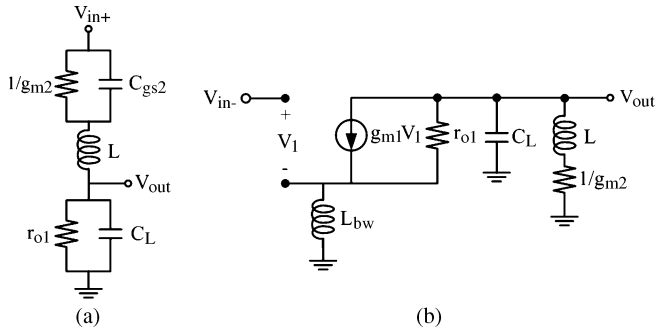

Fig. 11. Equivalent circuit model of the D-to-S amplifier (a) from Vin+ (b) from Vin-.

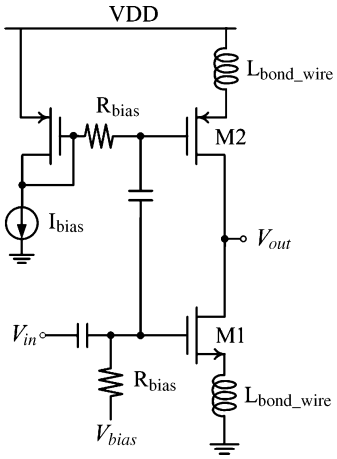

Fig. 12. Schematic the wideband power amplifier.

follower (M2). Due to the unequal amplification of the positive and negative paths, the differential-to-single-ended conversion does not double the signal swing.

The equivalent circuit of the D-to-S amplifier is shown in Fig. 11. From the viewpoint of the incoming signal Vin+, the behavior of the D-to-S amplifier acts as a source follower. On the contrary, from the viewpoint of the incoming signal Vin-, the D-to-S amplifier performs a common source amplifier with an inductive shunt peaking load. The M2 forms an equivalent resistor with resistance of 1/gm2 to reduce quality factor of the inductor for enlarge bandwidth. To equalize gain of the two paths from 3 to 8 GHz, the following equation should be sustained:

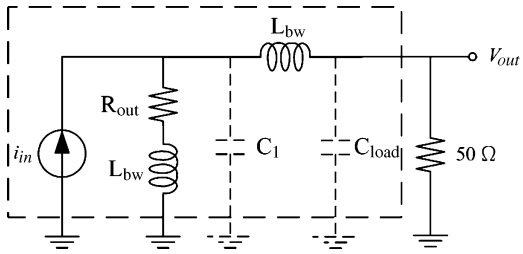

Fig. 13. Effective model of the power amplifier.

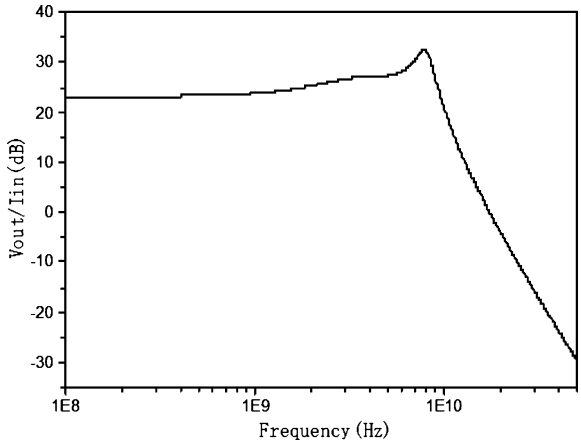

Fig. 14. Simulated frequency transfer function of the power amplifier.

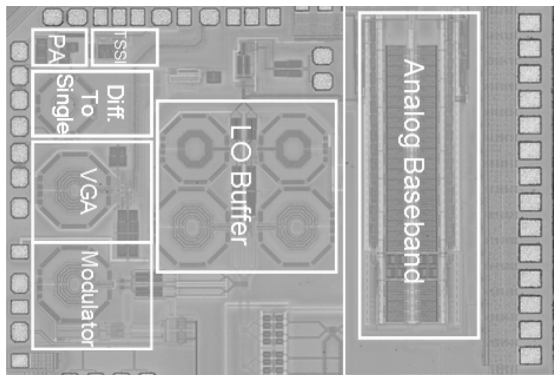

Fig. 15. Photograph of the chip.

$$\left|\frac{r_{o1}//\frac{1}{S\cdot C_L}}{\frac{1}{S\cdot C_{gs2}}//\frac{1}{g_{m2}}+S\cdot L+r_{o1}//\frac{1}{S\cdot C_L}}\right| = \left|\frac{g_{m1}}{1+S\cdot L_{bw}\cdot g_{m1}}\cdot\left(\frac{1}{g_{m2}}+S\cdot L\right)\right|. \quad (8)$$

Where C_L is output loading capacitor, $L_{\rm bw}$ is bonding wire connected between source of M1 and ground. r_{o1} is output resistance of M1, g_{m1} and g_{m2} are trans-conductance of M1 and M2, respectively. Ideally, the output of source follower is equal phase to the input and the output of common source amplifier has 180 degree phase rotation from input. Therefore, the incoming signals Vin+ and Vin- will be in-phase at output of the D-to-S amplifier. But the parasitic capacitors and on-chip inductor cause

Fig. 16. Measured frequency response of the analog baseband.

Fig. 17. Measured output return loss of the transmitter.

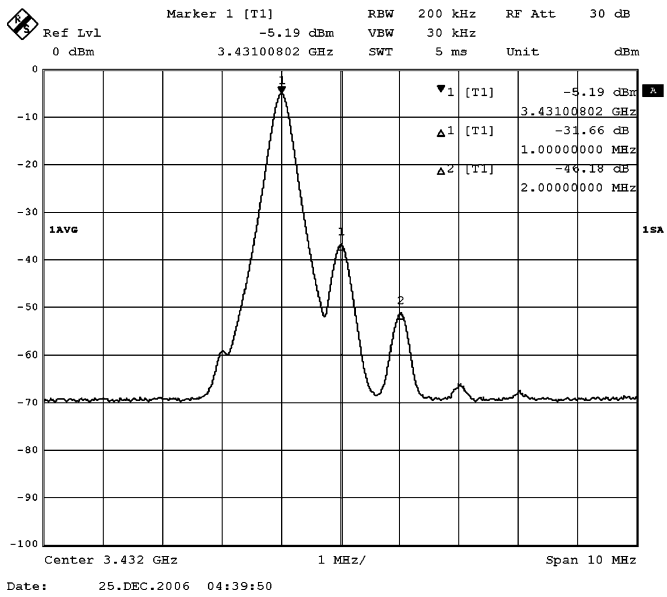

Fig. 18. Measured output power, carrier suppression, and sideband suppression performance at 3432 MHz.

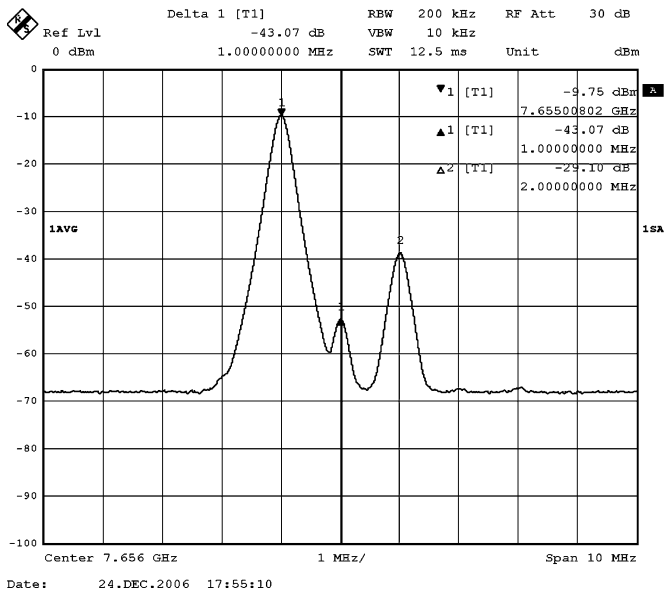

Fig. 19. Measured output power, carrier suppression and sideband suppression performance at 7656 MHz.

phase rotation as they are charged and discharged by signals. The inductor causes opposite phase rotation from the parasitic capacitors, which compensates phase error caused by the parasitic capacitors. Therefore, by post-simulation, a gain error of 1 dB and a phase error of 10 degree are obtained up to 8 GHz by careful choosing size of MOS transistors (M1–M2) and on-chip inductor. The error is acceptable in this design. The inductance of the on-chip inductor is 2 nH. The power consumption of the D-to-S amplifier is 8 mW.

In design of the power amplifier (PA), it is difficult to achieve high linearity and a broadband output matching across 3–8 GHz, as well as low power consumption simultaneously. Three approaches have been commonly used for broadband PA design, including filter theory design, distributed amplifiers and resistive shunt-feedback [6]. Using filter theory design, LC-based networks help achieve wideband matching. However, multiple LC stages might be necessary to cover broad bandwidth such that they usually occupy a substantial die area. Distributed amplifiers have high linearity, but their power consumption and occupied area can be quite high. In the approach of resistive shunt-feedback, the feedback resistor can lead to gain degradation.

To overcome these difficulties, the proposed power amplifier is realized by CMOS (both pMOS and nMOS) configuration, as shown in Fig. 12. By using appropriate transistor sizes, the parallel combination of the nMOS and pMOS transistors provides a low output resistance, which is wideband conducive to 50 Ω. The equivalent output resistance of the power amplifier (Rout) is $r_{\rm op}//r_{\rm on}$. The equivalent model of the power amplifier is shown in Fig. 13. C_1 is parasitic capacitance as

$$C_1 = C_{bp} + C_{d1} + C_{d2}. \tag{9}$$

$C_{\rm bp}$ denotes the parasitic capacitance of a bonding pad. C_{d1} and C_{d2} are drain capacitor of M1 and M2, respectively. In the model, bonding wires $(L_{\rm bw})$ connected to the equivalent output resistance $(R_{\rm out})$ form an inductive shunt peaking load. Let

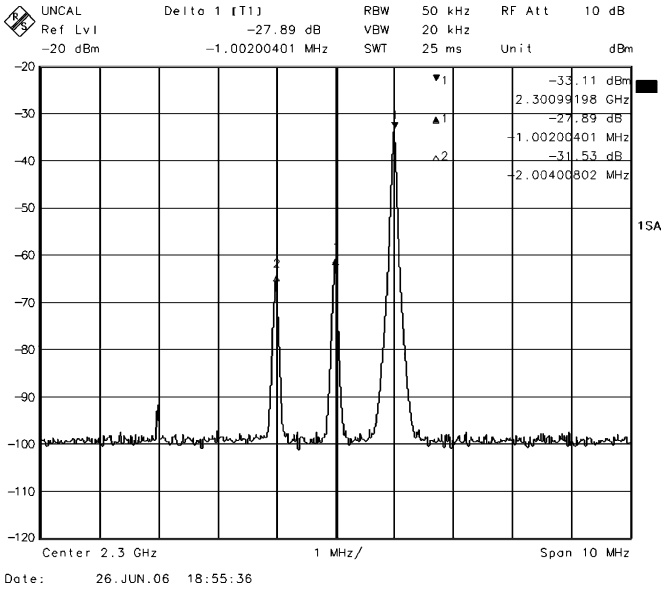

Fig. 20. Measured output spectrum at 2.3 GHz.

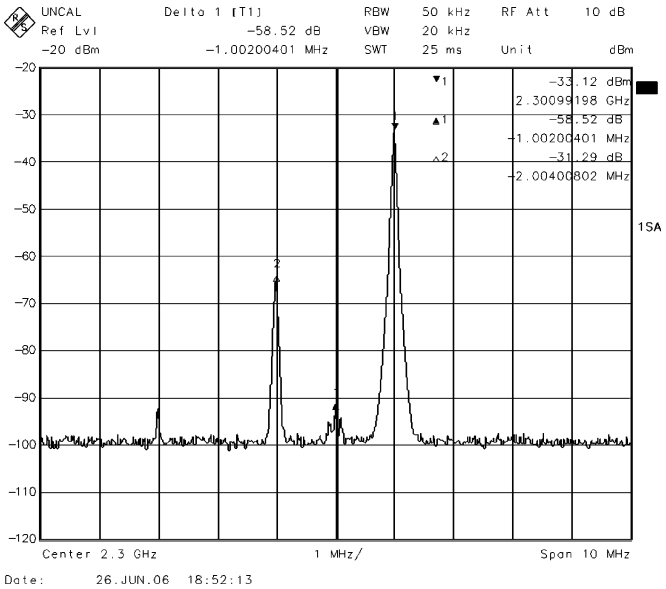

Fig. 21. Measured output spectrum at 2.3 GHz after calibration.

$L_{\rm bw} = 1$ nH, $C_1 = C_{\rm load} = 1$ pF and $R_{\rm out} = 50\ \Omega$. The simulated frequency transfer function peaks at 8 GHz to extend operation frequency of the power amplifier, as shown in Fig. 14. The power consumption of the power amplifier is 18 mW.

IV. Experimental Result

The UWB RF transmitter is implemented in a 1.2 V 0.13-μm CMOS process. The photograph of the chip is as shown in Fig. 15. The RF circuits and the analog baseband occupy an active area of 1.2×0.4 mm^2 and 0.9×0.35 mm^2, respectively. The following measurement results are based on the bias condition of current consumption of 55 mA from a 1.2 V supply. Fig. 16 shows the measured frequency response of the analog baseband with bandwidth of 250 MHz. The output impedance of the transmitter was matched to 50 Ω over 3–8 GHz. As shown in Fig. 17, the measured output return loss

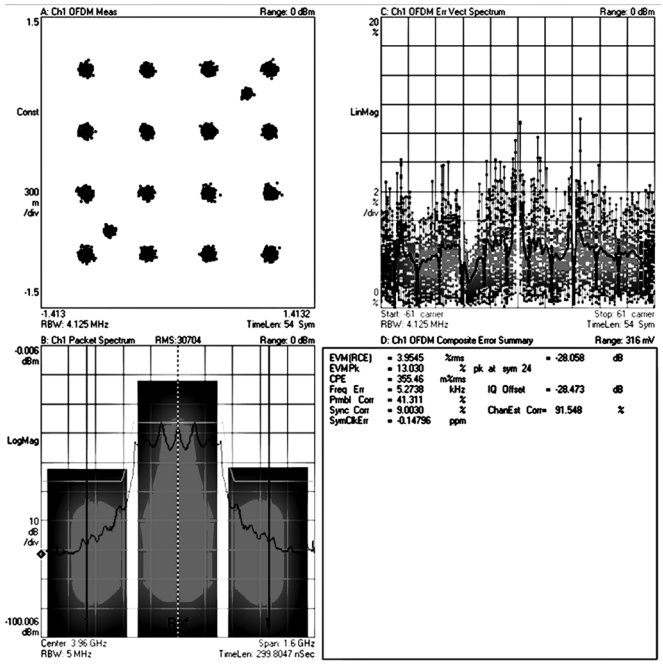

Fig. 22. Measured EVM under a data rate of 480 Mbps in MB-OFDM modulation.

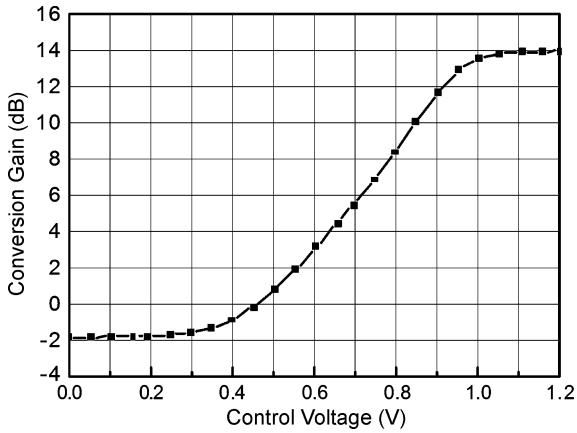

Fig. 23. Measured gain tuning characteristic of RF VGA.

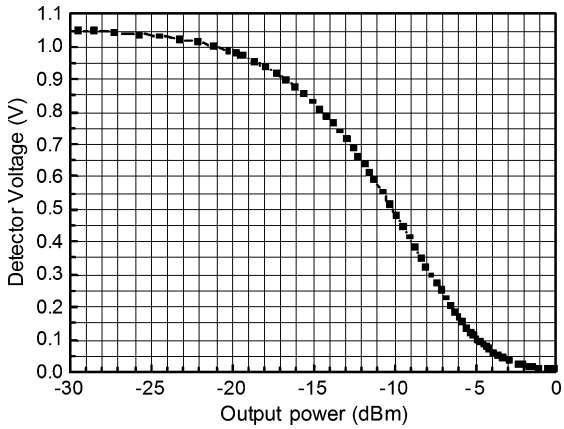

Fig. 24. Measured transmitted power sensing characteristic of TSSI.

is better than −9.3 dB in the frequency range of 3–10 GHz. The IQ modulation accuracy is demonstrated by the parameters of sideband, carrier suppression and error vector magnitude

TABLE III
PERFORMANCE SUMMARY

	3432MHz	3960MHz	4488MHz	6600MHz	7128MHz	7656MHz
$P_{out,max}$ (dBm)	-5.17	-5.36	-6.06	-6.3	-8.8	-9.71
OP1dB (dBm)	1.5	1.3	1.7	0.2	0.4	-0.6
Sideband Suppression (dBc)	46.1	43.7	40.4	30.4	30.1	29.1
Carrier Suppression (dBc) (before calibration)	31.6	29.4	27.6	21.0	25.5	43.7

TABLE IV
PERFORMANCE COMPARISON

	[7]	[8]	[9]	This work	
Frequency range (Hz)	3-9.5 G	3-8 G	3-8 G	3-8 G	
$P_{out,max}$ (dBm)	N.A.	N.A.	N.A.	-5 (3.4 G)	-9.7 (7.6 G)
Linearity (dBm)	-2.8 (OP1dB)	N.A.	-8.2 to -6.8 (OIP3)	1.5 (OP1dB) (3.4 G)	-0.6 (OP1dB) (7.6 G)
Sideband Suppression (dBc)	N.A.	N.A.	42.2-43	46 (3.4 G)	29 (7.6 G)
Carrier Suppression (dBc)	N.A.	-70 dBm (3.4 G)	46.5-47.3	31.6 (3.4 G)	43.7 (7.6 G)
EVM (dB)	-28	-28	-25.3	-28	
Dynamic range (dB)	N.A.	N.A.	N.A.	14 (linear-in-dB)	
Power Consumption (mW)	131 (Tx mode, including Sx)	Tx chain: 45.6 LO generator (excluding PLL): 62.4	IQ DAC: 81 Tx w/o DAC: 36 Sx: 102.6	Analog BB	10
				IQ Mod (+DACs)	4+0.6
				RF VGA	8
				D-to-S Amp	8
				Power Amp	18
				LO Buffer	16.2
				TSSI	1.2
				Total	66
Supply Voltage (V)	1.1 V	1.2 V	1.8 V	1.2 V	
Technology (CMOS)	90 nm	65 nm	0.18 μm	0.13 μm	

(EVM). In Fig. 18, the measured output power, sideband and carrier suppression (before calibration) at frequency of 3432 MHz are −5.1 dBm, 46.1 dBc, and 31.6 dBc, respectively. In Fig. 19, the measured output power, sideband and carrier suppression (before calibration) at the frequency of 7656 MHz are −9.7 dBm, 29.1 dBc, and 43 dBc, respectively. The uncalibrated carrier leakage data are used to show performance limitation of design consideration in Section III-B. Table III summarizes the measured output power, OP1 dB, sideband suppression and carrier suppression (before calibration) for each frequency from 3.4 to 7.6 GHz. An out-off-band frequency response has also been measured at 2.3 GHz, as shown in Fig. 20. The measured result shows the output power degrades from −5.1 dBm (at 3.432 GHz) to −33.11 dBm (2.3 GHz). The output power degradation is contributed both by band-pass response of IQ modulator, RF VGA, D-to-S amplifier and power amplifier. The

performance of digital-assisted carrier leakage calibration also demonstrates after the out-off-band measurement. Before performing the calibration, as shown in Fig. 20, the measured carrier leakage is 27.89 dBc. After performing the calibration, as shown in Fig. 21, the measured carrier leakage is 58.52 dBc has. There is an improvement of 30.63 dB by the calibration. In Fig. 22, the measured EVM is -28 dB under the data rate of 480 Mbps in MB-OFDM modulation as output power of -10 dBm at 3960 MHz. The measured tuning characteristic of RF VGA and sensing characteristic of TSSI are shown in Fig. 23 and Fig. 24, respectively. In Fig. 23, the RF VGA provides gain tuning range of 14 dB. In Fig. 24, the TSSI has linear power detection range from -20 to -5 dBm. Table IV summaries the performance of this work and compares with the reported UWB transmitters.

V. Conclusion

A highly-integrated RF transmitter with features of wide-bandwidth, high linearity and high modulation accuracy for UWB has been presented. A digital-assisted carrier leakage calibration effectively reduces the carrier leakage associated with DC-offset of the IQ modulator. An automatic transmit power control is adopted to control the transmitted power precisely for maximizing the link quality and avoiding to interfere other communication systems. The chip occupies 0.795 mm^2 and consumes 66 mA in a 1.2 V 0.13 μm CMOS process.

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