A 2.24 mW 74 dBΩ-Gain, dc to 600 MHz-BW Differential Baseband Amplifier for 60 GHz Wireless Applications

Horng-Yuan Shih, *Member, IEEE*, Chun-Fan Chen, and Sheng-Kai Lin

***Abstract*—A low power, wideband and high linearity current-mode based differential baseband amplifier with a bandwidth from dc to 600 MHz applied for 60 GHz zero-IF RF receiver is presented. The wideband differential baseband amplifier is realized in a 90 nm CMOS process. A series-series feedback technique and a Q-enhanced active inductor are adopted in the current-mode baseband amplifier for achieving wideband and high linearity under a small current consumption. The measured maximum BW of 600 MHz, gain of 74 dBΩ and OIP3 of $+12.5$ dBV are realized with power consumption of only 2.24 mW under a supply voltage of 1.4 V. The measured performance shows the baseband amplifier fulfills the requirements for 60 GHz zero-IF RF transceivers.**

***Index Terms*—Analog baseband, current amplifier, low power, ultra wideband (UWB).**

I. Introduction

THE 60 GHz ultra-wideband (UWB) systems are applied in short range and high speed wireless communications for realizing data rate of several Gb/s. Data rate of beyond Gb/s results in wide bandwidth requirement of the baseband circuits. To realize a data rate up to 1 Gb/s by a zero-IF receiver, the required bandwidth of the analog baseband is at least 500 MHz. Moreover, the receiver should provide a gain of at least 58 dB for boosting the received signal to 0 dBm under a 1 m link [1]. As front-end offering a gain of 20 dB, analog baseband is required to provide a gain of 38 dB. Otherwise, using a high spectrum efficient modulation scheme like 16QAM or 64 QAM, the analog baseband is needed to be high linearity for maintaining SNR. Therefore, for the design of the wideband analog baseband applied for 60 GHz UWB systems, bandwidth, gain, linearity, noise and power consumption should be trade-off for fulfilling the system requirements. Several previous works had realized the required wideband analog baseband applied for receivers of 60 GHz UWB systems [2], [3]. All of those designs implement the wideband analog baseband in voltage-mode circuits. For processing voltage signals in the voltage-mode circuits, nodes in the voltage-mode circuits present high impedance. Consequently, realizing a wideband and high linearity analog baseband by the voltage-mode circuit leads to high power consumption. On the contrary, owing to processing signals in current domain, nodes in current-mode circuits present low impedance. Therefore, the current-mode circuits can achieve wideband and high linearity under much smaller power consumption than voltage-mode circuits. Active inductors have been widely used in voltage-mode circuits for extending bandwidth. In this design, by using both of series-series feedback technique and Q-enhanced active inductors, a current-mode differential baseband amplifier with maximum BW of 600 MHz, gain of 74 dBΩ and OIP3 of $+12.5$ dBV under power consumption of only 2.24 mW is proposed for 60 GHz UWB systems.

Manuscript received September 25, 2012; revised January 08, 2013; accepted January 27, 2013. Date of publication February 13, 2013; date of current version March 07, 2013.

The authors are with the Department of Electrical Engineering, Tamkang University, Tamsui, New Taipei 25137, Taiwan (e-mail: hyshih.tw@gmail.com).

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Digital Object Identifier 10.1109/LMWC.2013.2244874

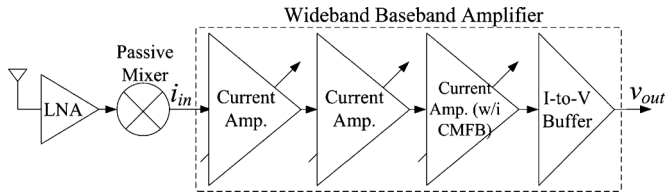

Fig. 1. Proposed 60 GHz UWB zero-IF receiver.

II. System Architecture

A proposed 60 GHz UWB zero-IF receiver is shown in Fig. 1. The receiver is consisted of a low noise amplifier (LNA), a down-conversion mixer and a wideband baseband amplifier. The down-conversion mixer is implemented by a passive-mixer for good linearity and reducing current consumption. Owing to that output baseband signals of the passive mixer is a wideband ac current, a current-mode differential baseband amplifier is proposed for amplifying the baseband signals. As shown in Fig. 1, the current-mode baseband amplifier is composed of two current amplifiers, a current amplifier with output common-mode feedback (CMFB) circuits and an I-to-V buffer.

III. Circuit Design

The schematic of the proposed differential current amplifier is shown in Fig. 2(a). The input stage of the current amplifier is in the common-gate (CG) configuration with a series-series feedback circuit (M1-M4) for achieving low input resistance (50 Ω) and parasitic capacitance with small-size transistors bias under a small current consumption [4]. The second stage of the current amplifier is a cascode current mirror (M2, M5 and M6) with an active load (M7). Current gain of the current amplifier is determined by the size ratio between M2 and M5. For achieving wide bandwidth and high linearity, the input capacitance of the cascode current mirror should be minimized [5]. Owing to using small-size transistors for M1 and M1b and biasing M1 and M1b under a small bias current, the cascode current mirror (M2, M2b, M5 and M5b) can be designed in small-size transistors, which

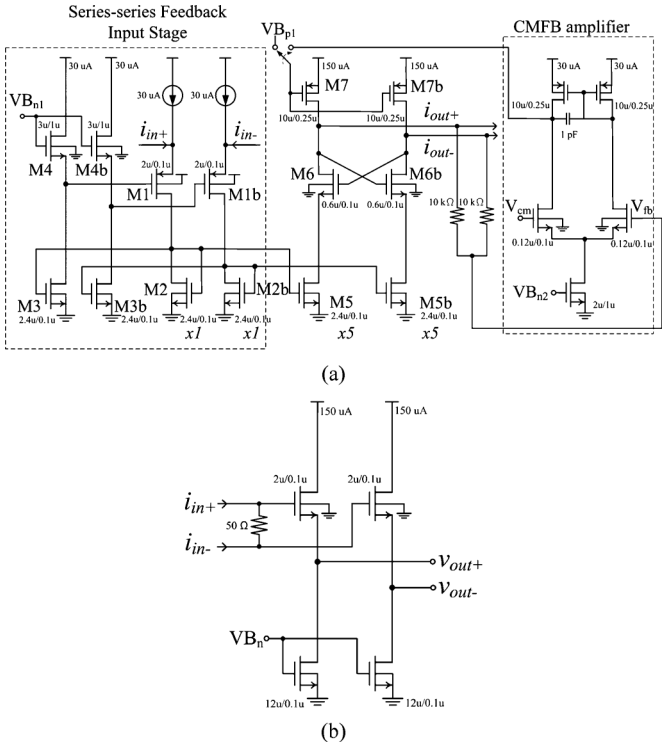

Fig. 2. (a) Proposed differential current amplifier. (b) I-to-V buffer.

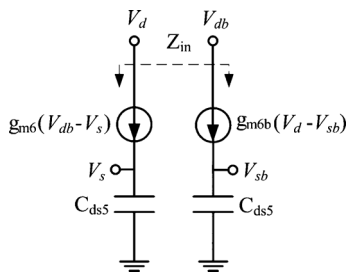

Fig. 3. Equivalent circuit of the cascode current mirror.

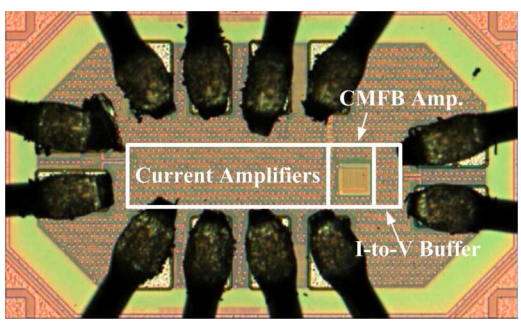

Fig. 4. Chip micrograph of the baseband amplifier.

leads to small parasitic capacitance. Thus, the bandwidth and linearity of the current amplifier can be greatly improved.

The cascode stage (M6 and M6b) of the cascode current mirror is configured as a cross-coupled pair for performing a Q-enhanced active inductor to improve bandwidth of the current amplifier. The equivalent circuit of the cascode current mirror is shown in Fig. 3. The output impedance of the cascode current mirror can be derived as

$$Z_{\mathrm{in}}(\omega) \approx \frac{-2}{g_{m6}} + j\frac{2}{\omega \cdot C_{ds5}} \tag{1}$$

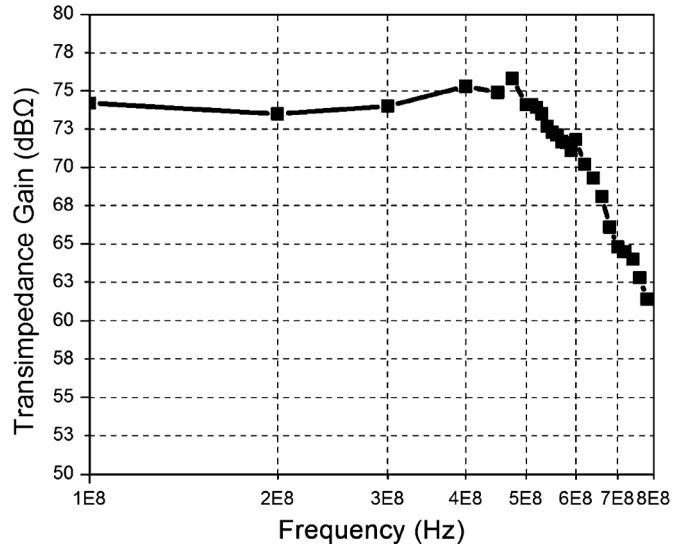

Fig. 5. Measured frequency response of the wideband baseband amplifier.

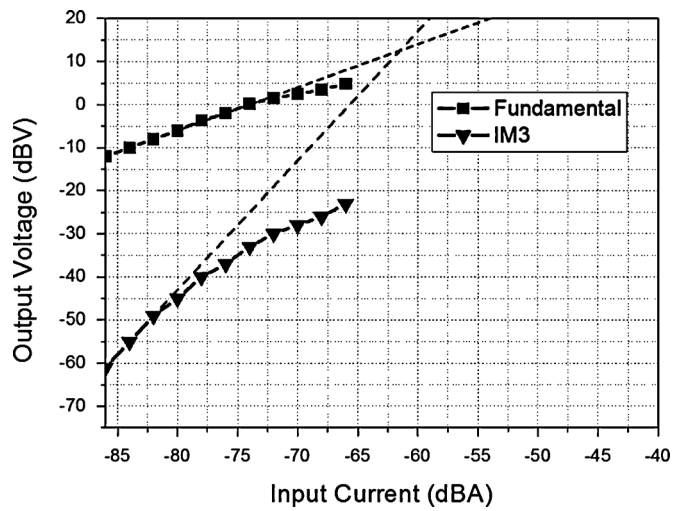

Fig. 6. Measured linearity performance of the baseband amplifier.

where g_{m6} is trans-conductance of the cross-coupled pair (M6 and M6b). C_{ds5} is the total parasitic capacitance at source of the cross-coupled pair (M6 and M6b). The output impedance of the current amplifier can be derived as

$$Z_o(\omega) \approx \frac{2r_{o7}\left(\frac{g_{m6}}{C_{ds5}}\right)^2}{\left(\frac{g_{m6}}{C_{ds5}}\right)^2 - g_{m6}r_{o7}} \Big/\!\Big/ j\frac{1}{\omega\left[\frac{C_{ds5}}{2} - 2(C_{dg6}+C_{ds7})\right]} \tag{2}$$

where r_o is the output resistance of the active load (M7). $2(C_{dg6} + C_{ds7})$ is the total parasitic capacitance at the differential output nodes. According to (2), the negative resistance of the cascode current mirror can be used to enlarge the output resistance of the current amplifier. Besides, the inductive reactance of the cascode current mirror resonates with the total parasitic capacitance at the differential output nodes for extending bandwidth.

A current amplifier with output common mode feedback (CMFB) serves as the last stage of the wideband analog baseband before the I-to-V buffer. In the first and the second

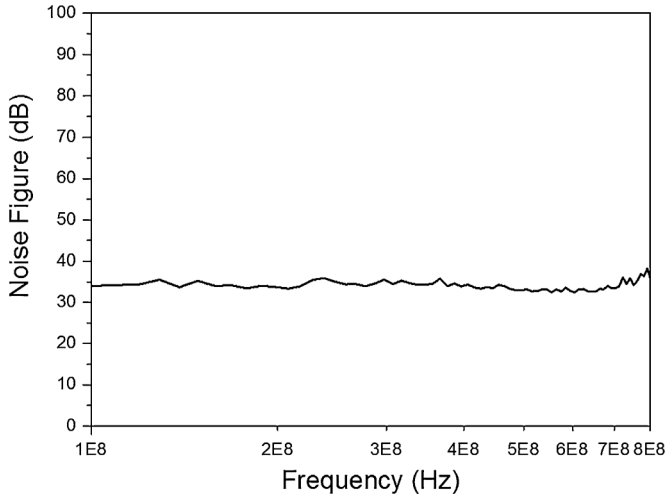

Fig. 7. Measured noise figure of the baseband amplifier.

TABLE I
PERFORMANCE SUMMARY

	This Work	[4]	[2]	[3]
Bandwidth (f_{3dB})	600 MHz	250 MHz	915 MHz	900 MHz
Max. Gain	74 dBΩ (Voltage Gain: 40 dB)	107 dBΩ (Voltage Gain: 73 dB)	Voltage Gain: 20 dB	Voltage Gain: 33 dB
Linearity	-17.5 dBm (IIP3@Gain= 40 dB)	-6 dBV (OIP3@Gain =73 dB)	+8.2 dBm ((IIP3@Gain =0 dB)	-34 dBm ~ -18dBm (IP1dB)
Noise Figure	33 dB (IRN=-137.8 dBm/Hz)	14 dB (IRN=-156.8 dBm/Hz)	25.8 dB (IRN=-145 dBm/Hz)	11 dB (IRN=-159.8 dBm/Hz)
Filter Order	4th-order	6th-order Chebyshev	6th-order	3rd-order Butterworth
Gain Tuning Range	No	82 dB	20 dB	29.4 dB
Power Consumption	2.24 mW	60 mW	9.5 mW/10.8 mW	29.76 mW (I/Q)
Technology	90 nm CMOS	0.13 μm CMOS	90 nm CMOS	65 nm CMOS
FOM	42.93	0.62	12.97	9.18

FOM is defined by (IIP3(dBm)+Gain(dB)-IRN(dBm/Hz))* BW(GHz) / power consumption (mW). For [3], IIP3=IP1dB+10dB.

current amplifier of the analog baseband, the output dc level is defined by the input stage of the next current amplifier. Unlike the first and the second current amplifier, the last current amplifier designed in the baseband amplifier needs a common mode feedback circuit for defining it's output dc voltage. The schematic of the current amplifier with CMFB is also shown in Fig. 2(a). A common mode feedback amplifier is adopted to adjust the output dc voltage $(\mathrm{V_{fb}})$ of the current amplifier to a pre-determined voltage $(\mathrm{V_{cm}})$ through the active load of the current amplifier. Schematic of the I-to-V buffer is shown in Fig. 2(b). The I-to-V buffer is cascaded by a 50 Ω resistor used for converting the output signal from a current to a voltage under wide bandwidth and a source follower used to play a role of buffer for the purpose of measurement.

Owing to the high output impedance of the passive mixer, the input referred noise current of the current-mode baseband amplifier depends critically on the trans-conductance of M2 and the current source $(\mathrm{I_{SS}})$ of the first current amplifier [Fig. 2(a)], as indicated in the following equation:

$$\overline{i}_{n,\mathrm{in}}^2 \approx 4kT \cdot \gamma \cdot (g_{m2} + g_{mss}) \tag{3}$$

where γ is a process-relative coefficient. Consequently noise performance of the current-mode baseband amplifier directly depends on the current consumption.

IV. Experimental Results

Fig. 4 shows a die micrograph of the wideband baseband amplifier with a core size of $500 \times 260\ \mu\mathrm{m}^2$. Fig. 5 shows the measured frequency response of the wideband baseband amplifier. Owing to application of the Q-enhanced active inductor in the baseband amplifier, a gain-boosting at near 500 MHz can be obtained. The trans-impedance gain of 74 dBΩ is converted from measured voltage gain of 40 dB as input impedance is 50 Ω. The measured linearity performance of the baseband amplifier is showed in Fig. 6. The strength of input ac current is converted from the strength of the input voltage under input impedance of 50 Ω. A measured OIP3 of $+12.5$ dBV is achieved under voltage gain of 40 dB and power consumption of only 2.24 mW. Thus, as referred to input, the IIP3 of the baseband amplifier is -27.5 dBV (equals -17.5 dBm under input impedance of 50 Ω). Owing to that the input resistance of the analog baseband is 50 Ω, the noise performance of the baseband amplifier can be indicated by measured noise figure (NF). As shown in Fig. 7, the measured NF is 33 dB due to small current consumption. Therefore, input referred noise voltage of the baseband amplifier is 40.6 nV/$\sqrt{}$Hz (-137.8 dBm/Hz). By cooperating with a RF front-end which provided a voltage gain of 35.5 dB published in [6], a high sensitivity 60 GHz receiver can be achieved. The performance summary of the baseband amplifier is shown in Table I. As comparing with other works, this work achieves the highest voltage gain of 40 dB and the highest linearity of $+12.5$ dBV (OIP3) under smallest power consumption of 2.24 mW.

V. Conclusion

A low power, wideband and high linearity differential baseband amplifier proposed for 60 GHz UWB systems with measured maximum BW of 600 MHz, gain of 74 dBΩ and OIP3 of $+12.5$ dBV under power consumption of only 2.24 mW was presented in this letter. The measured performance shows the baseband amplifier fulfills the requirements for 60 GHz zero-IF RF transceivers.

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